Fundamentals and Analogies for Low-Power CMOS Image Sensor Design

Suat U. Ay *Ph.D, P.E.*

Associate Professor

Electrical and Computer Engineering

University of Idaho

06/27/2023 @ IEEE SSC&CAS Event, Columbus, OH

Outline

- **Introduction: Design-by-Analogy (DbA) for engineering design**
- **An analogy for analog/mixed-signal circuits**
- **Analogies leading to Supply Boosting Technique (SBT)**
  - Fundamental principles / assumptions and circuit blocks for SBT
- **Application examples of SBT**
  - Comparator
  - ADC
  - CMOS Image Sensor (CIS) Readout
- **Utilization of SBT in low-power/low-voltage CIS design,**
- **Conclusion**

Definition of Analogy

Merriam-Webster dictionary definition of ***analogy (noun)***

1. a: a comparison of two otherwise unlike things based on resemblance of a particular aspect

b: resemblance in some particulars between things otherwise unlike: **Similarity**

2: **inference** that if two or more things agree with one another in some respects they will probably agree in others

"This is us."

Source: Andrew Toos, 2013 CartoonStock.com

Design-by-Analogy (DbA)

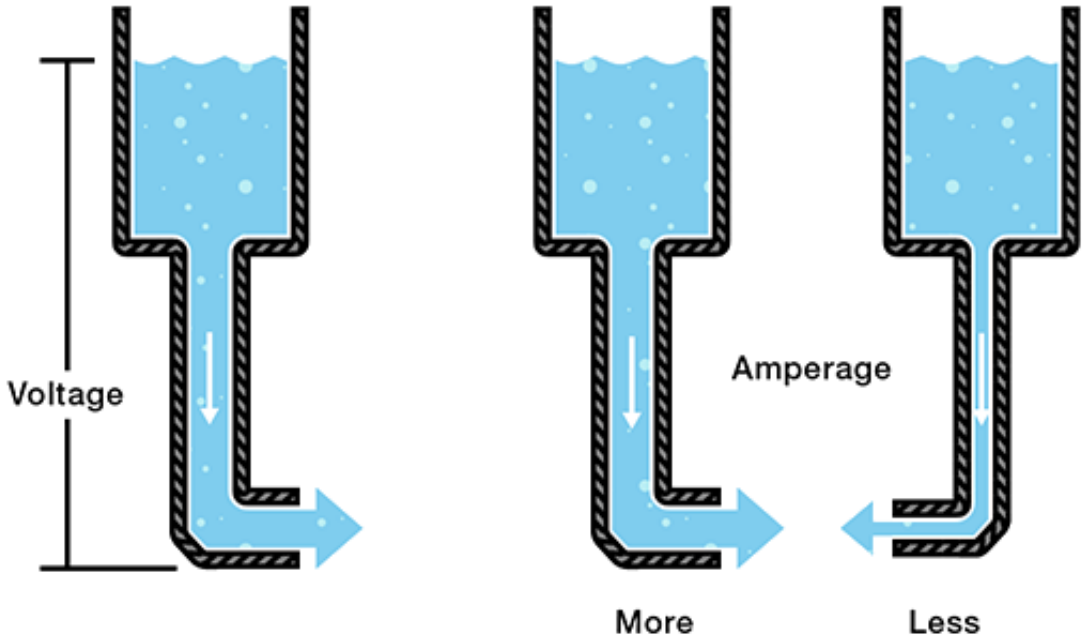
- DbA is an (engineering) design methodology;
  - New and innovative solutions are generated in a target domain (i.e. engineering, circuit design) based on inspiration drawn from a source domain (i.e. nature, life, society, etc.) through cross-domain analogical reasoning,
  - It helps designers
    - to generate patentable ideas and solutions, *(novel, non-obvious, useful)*
    - to mitigate design fixation, *(thinking out of the box)*
    - to improve design ideation outcomes,
    - to facilitate interdisciplinary contribution to a design.
- DbA methodology simply ***assumes*** that *similar problems can be solved by similar solutions from different domains!*

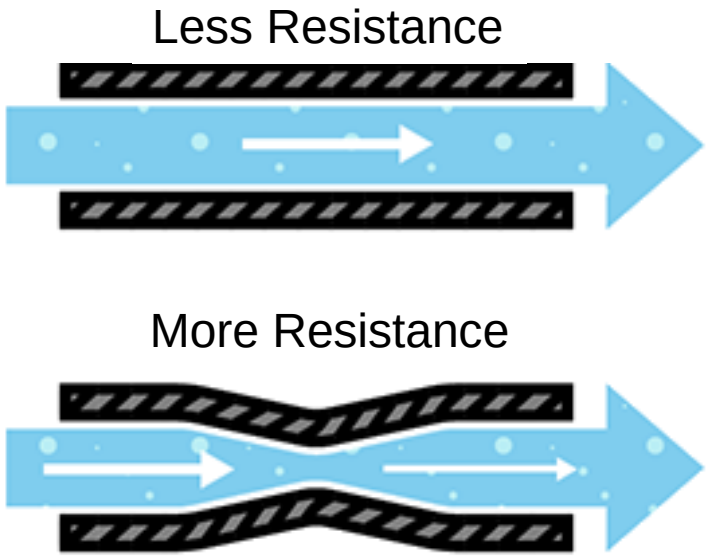
Analogy for Teaching Fundamentals

- We use analogies to teach engineering;
  - to simplify complex engineering facts and fundamentals,
  - to relate new knowledge to something everybody knows,
  - to maintain the knowledge longer,
  - to give different perspective
- Analogies in teaching science and engineering is considered as “two-edged sword”;
  - necessary to understand the extend of it’s use,
  - the “*personal construction of meaning*” depends on learners background & maturity

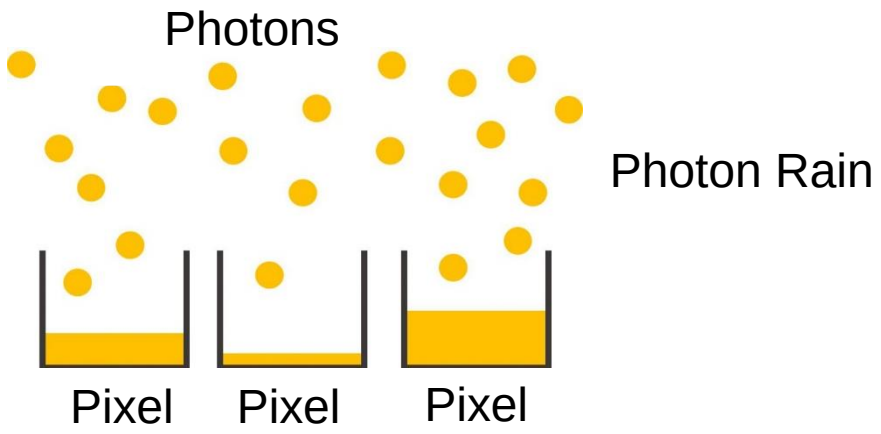
Use analogies in electrical engineering education

- **Water ←→ Electric current**



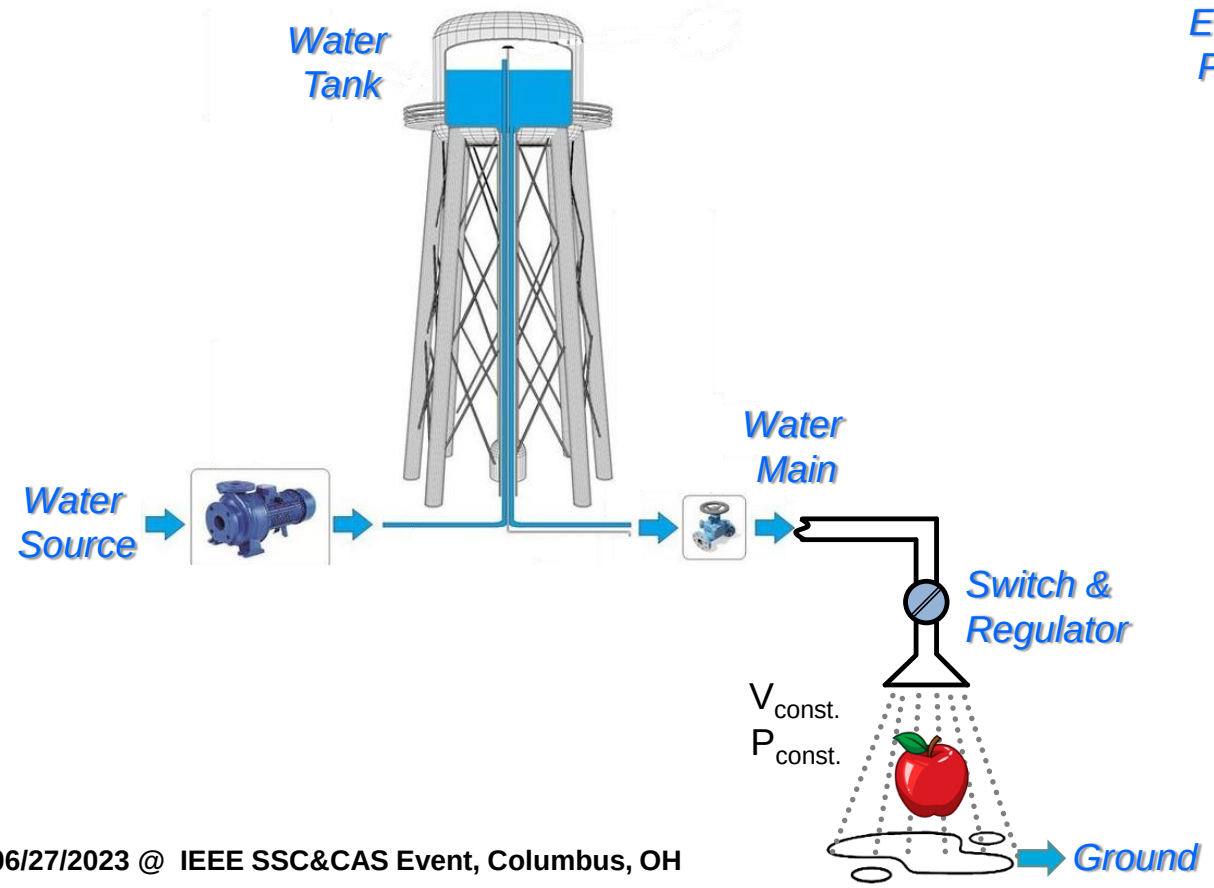


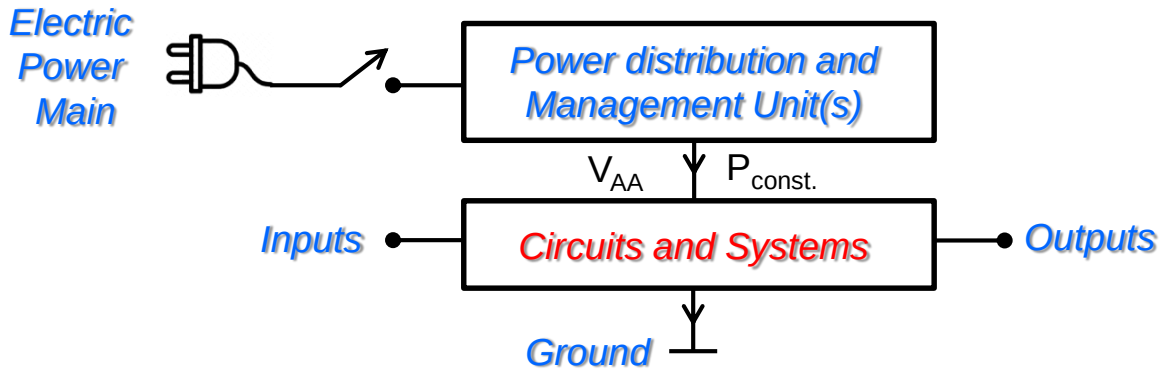
- **Photons ←→ Rain drops**



Water analogy for electrical circuits and systems

- Powering and operating of standard electrical circuits & systems resembles water distribution networks and how we use water in our daily life.



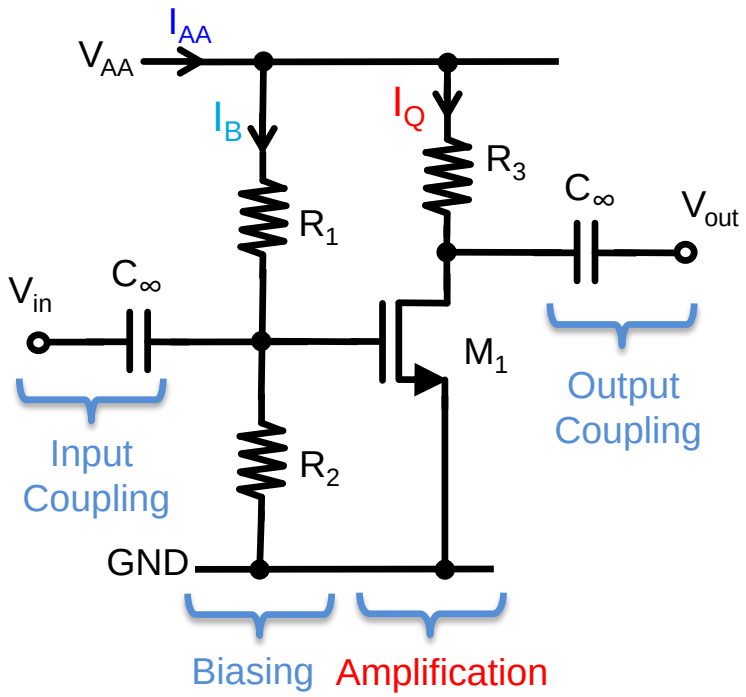


Assuming (Desired)

1. Power we used for the job (amplifying a signal or washing object/body/hand) is infinite,
2. Power (water pressure) and voltage (water volume) are regulated and constant,
3. Do not care about wasting! (or unaware!)

Powering/operating analog circuits

- What we know about circuit operations;
  - Almost all circuits we know/learned/use have powered continuously and have class-A biasing/operation!
- What is Class-A biasing/operation?



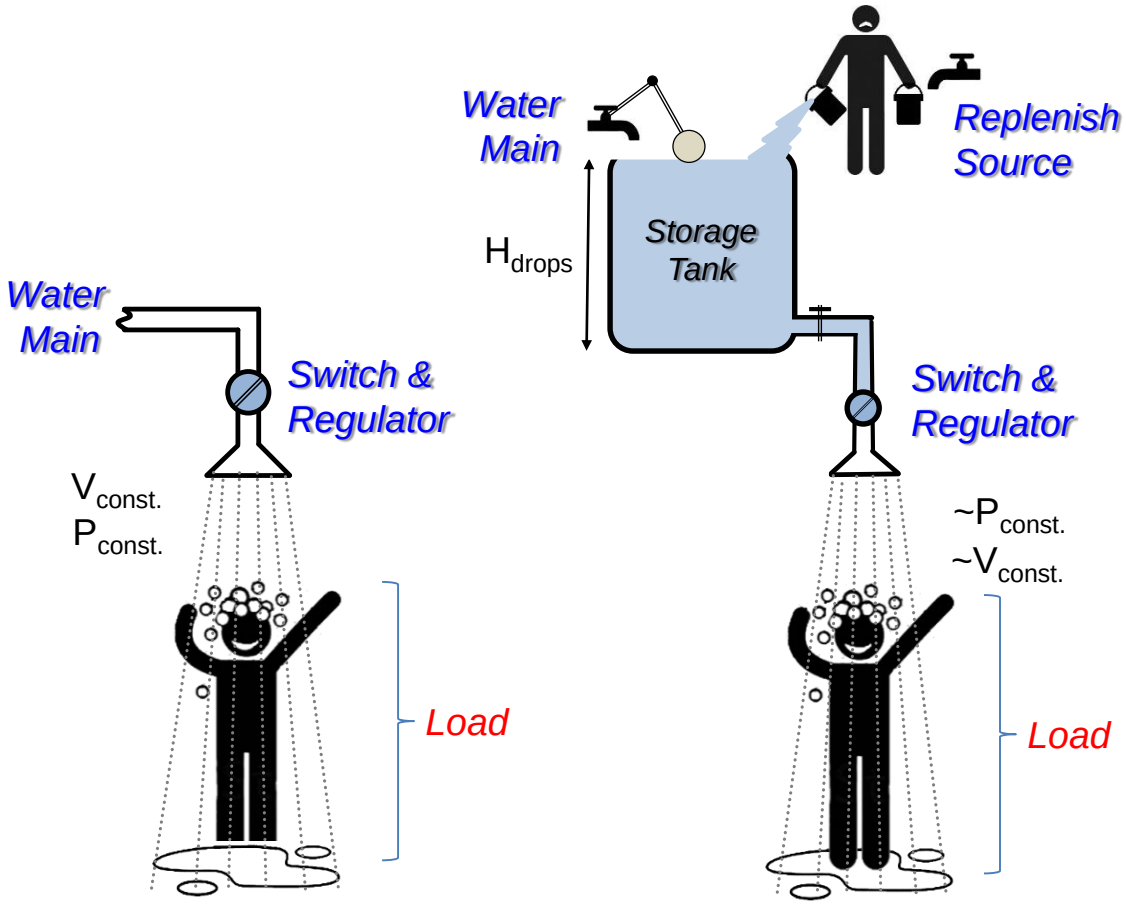
1- Active (Gain) element always works,
  * M_1 biased and kept in in “Saturation”,
  * I_Q current always runs,
  * I/O ranges defined by I_Q and M_1 size

2- Some other elements support active element(s),
  * R_1-R_3 to keep M_1 in saturation
  * Consume some power also (I_B<I_Q)
  * C_1&C_2 shapes input/output signals

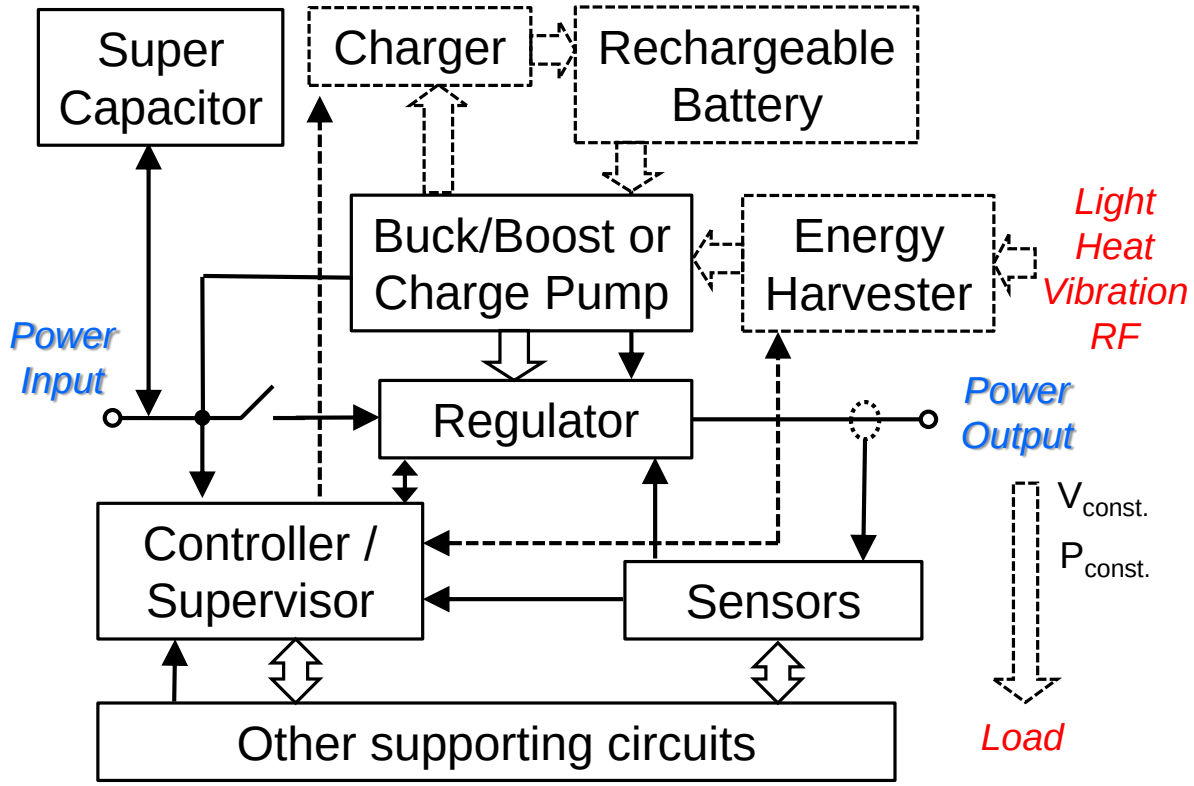
3- Power always consumed
  * if V_{in}=0, V_{out}=0 but I_B and I_Q are not
  * Efficiency (power) is input dependent and <<25%

Powering techniques for analog circuit

- Powering circuits today is like delivering water to a shower head…



Not much water loss, until it is used!



Lots of energy/power loss before load!

NOT Acceptable for energy/power limited cases!

Powering techniques under extreme source limited cases

- Require ultra-low power circuit design for self-powered systems,
- Analogy; my experience during early 1990's of Istanbul draught!

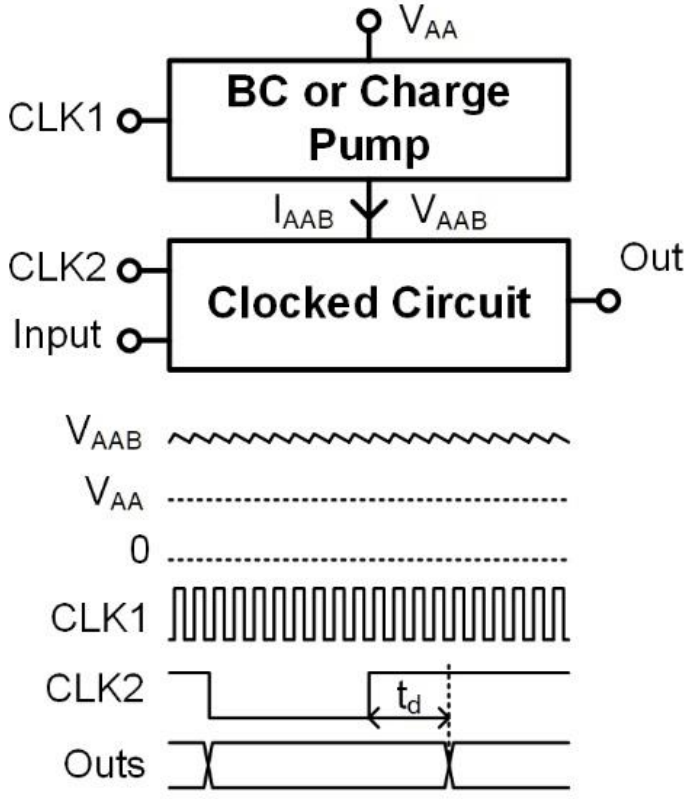
- Buy two 2 litres (~1.1gallon) bottled water,
- Worm them over panel radiator,
- Open several holes on the cups,
- Be mindful, careful, organized,
- Wash up before used all of the water!

I didn't care if the pressure or volume per pour was reduced, as long as I finished my shower before the water runs out!

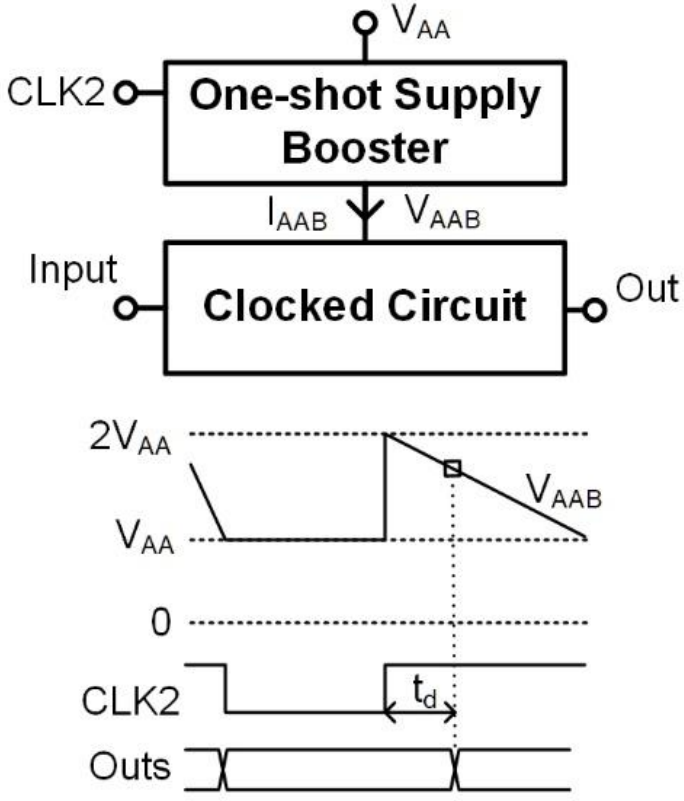
Very efficient way for powering and operating a circuit / system to get a job done!

Fundamentals : Supply Boosting Techniques

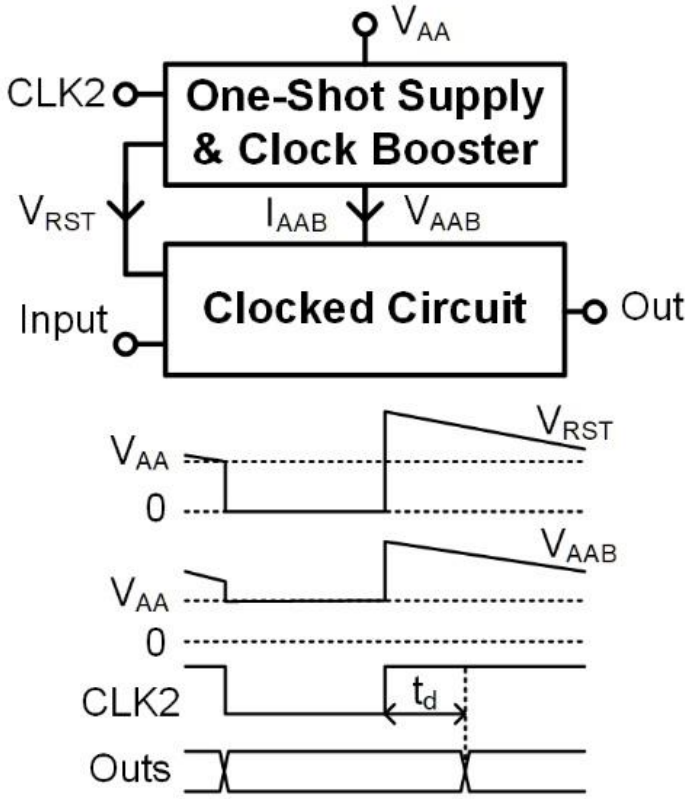
- Get the clocked operation completed before supply/clock drops unacceptable level.



Standard Supply Boosting Techniques



(One-Shot) Supply Boosting Technique

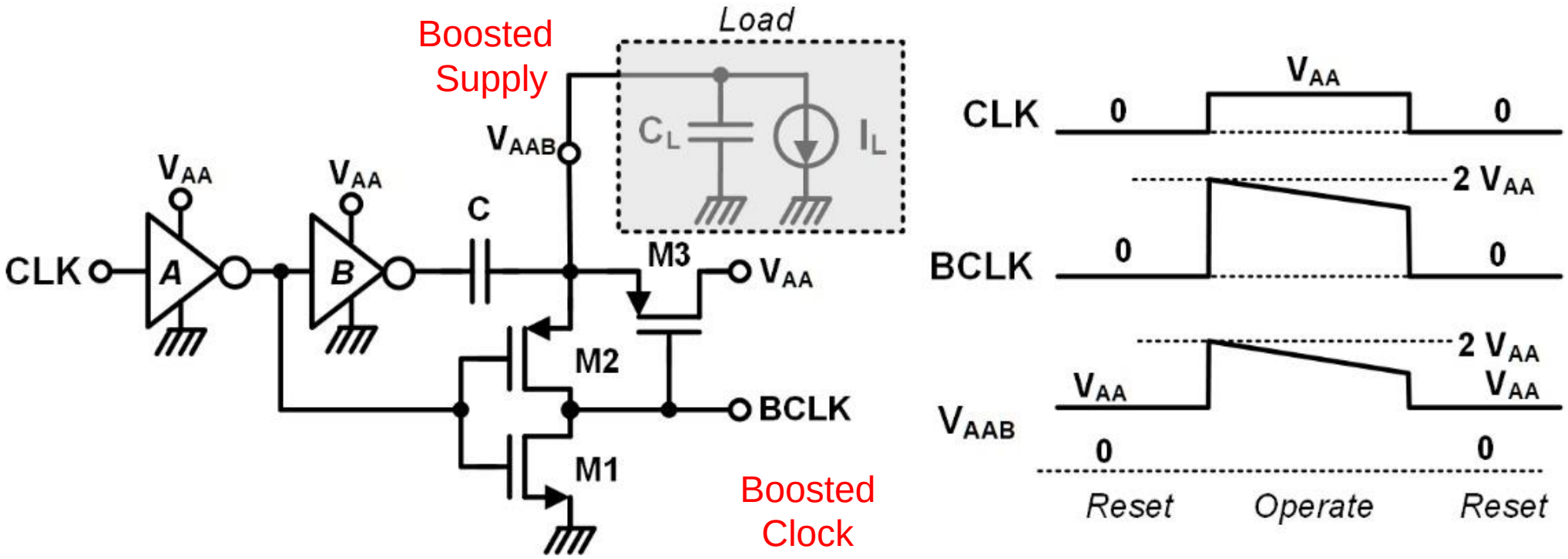


(One-Shot) Supply and Clock Boosting Technique

(One-Shot) Supply Boosting Techniques (SBTs)

- Get the clocked operation completed before supply/clock drops unacceptable level.
- Select a process that have higher process supply voltage than the system supply,
  - i.e. CMOS 0.5μm, 5V, 2P3M process (C5)
    - Process supply voltage (V_{AAP}) is 5V,
    - $V_{TH,N}$=+0.8V, $V_{TH,P}$= - 0.9V
    - Run your circuits at system supply voltage (V_{AA}), where : $V_{AA} < V_{AAP}/2$ (i.e. V_{AA}=1.2V)
- SBT can be used in pure analog operations too.
  - i.e. analog level shifting/buffering
    - Make sure very low-current is consumed during operation,
- Core circuit for the SBT is the supply/clocked booster (SCB) block
  - Has to be very simple and low leakage circuit,

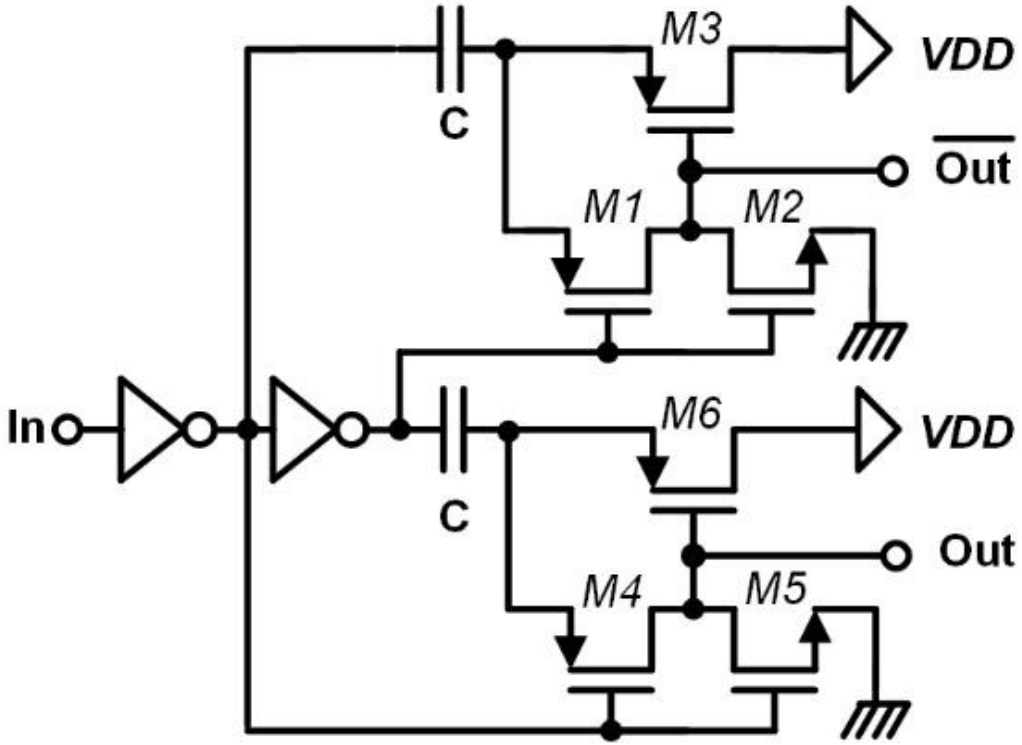
One-Shot Supply & Clock Booster (SCB) Circuit



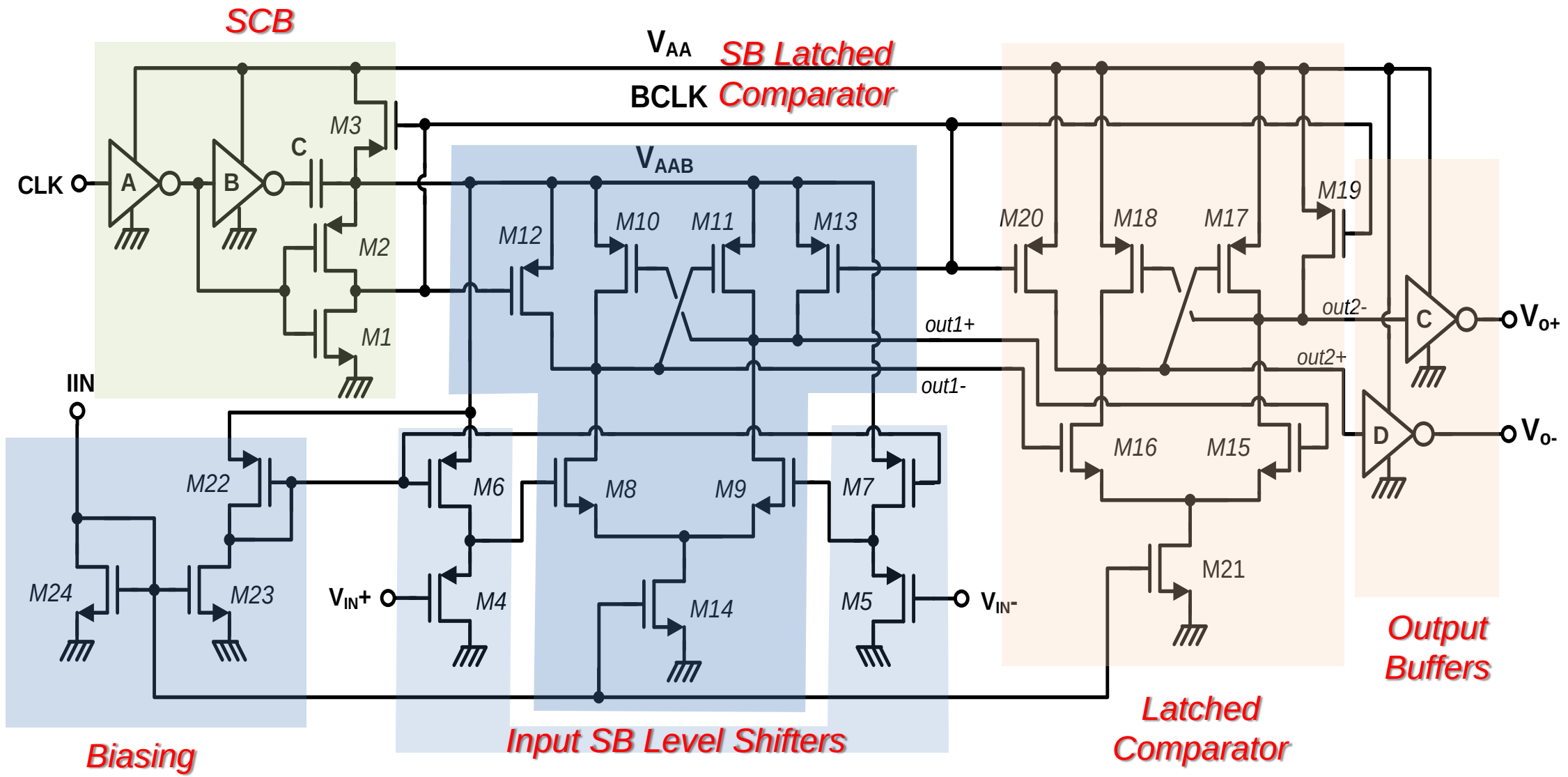
- Fill the boost capacitor once, discharge it during operation of the load (CLK=1).
- M3 prevents V_{AAB} to drop below V_{AA}
- No regulator (=no extra loss)

One-Shot Supply & Clock Booster (SCB) Circuit

Boosted Clock Buffer

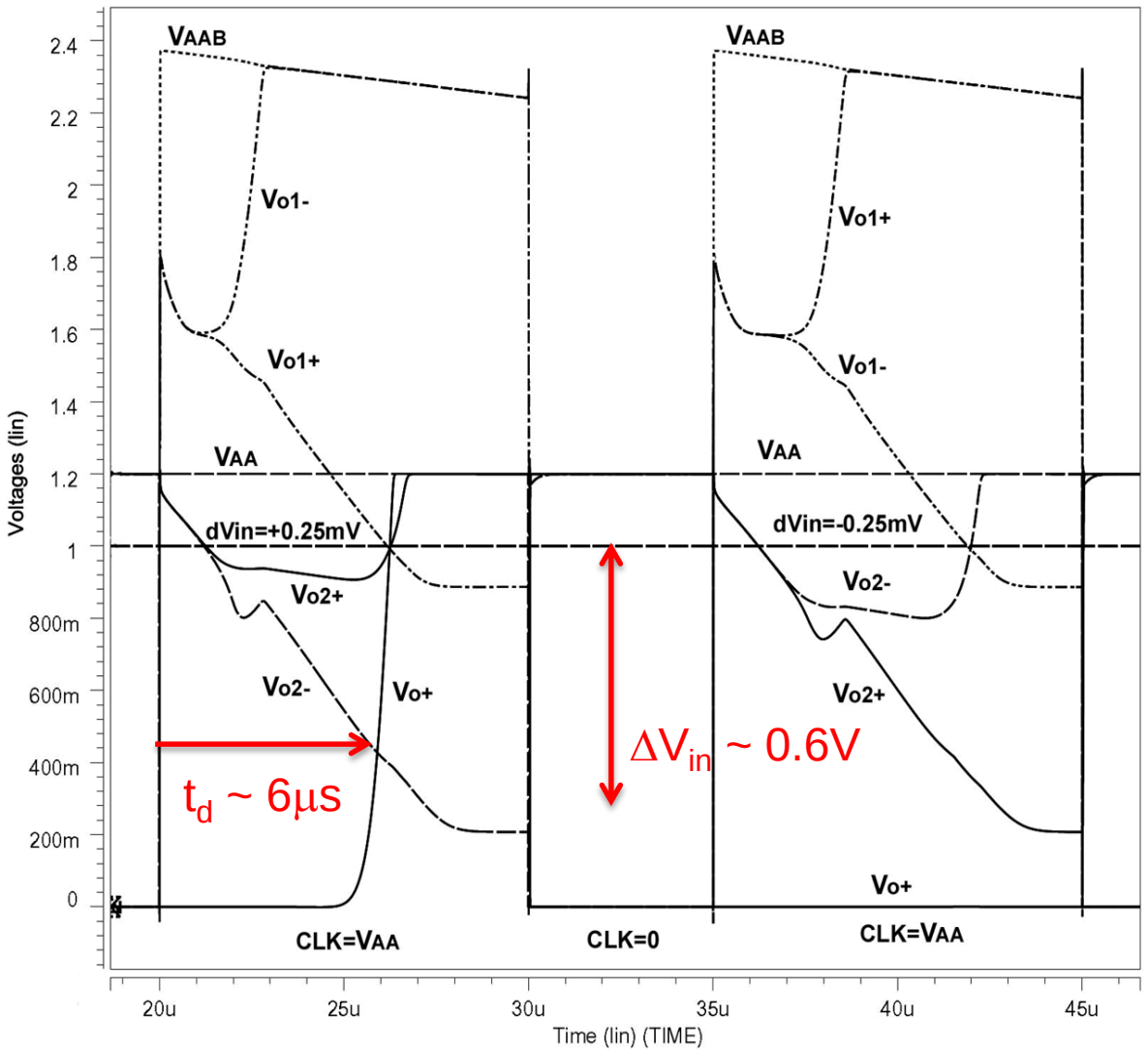


Supply Boosted Comparator (Rev.1)

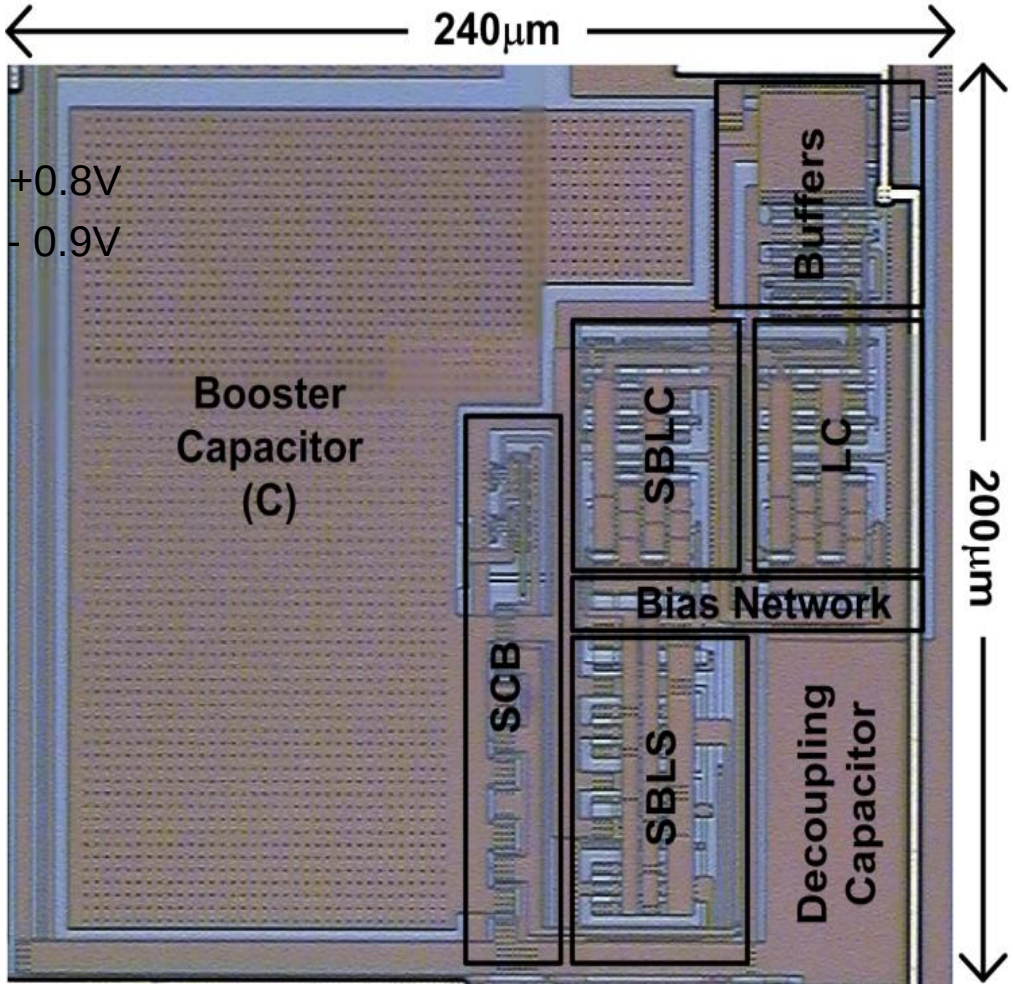


[1] Ay, S. U. "A sub-1Volt 10-bit Supply Boosted SAR ADC Design in Standard CMOS," Int. Journal on Analog Int. Circuits and Signal Proc., v.66, pp.213-221, 2010

Supply Boosted Comparator (Rev.1) – cont.



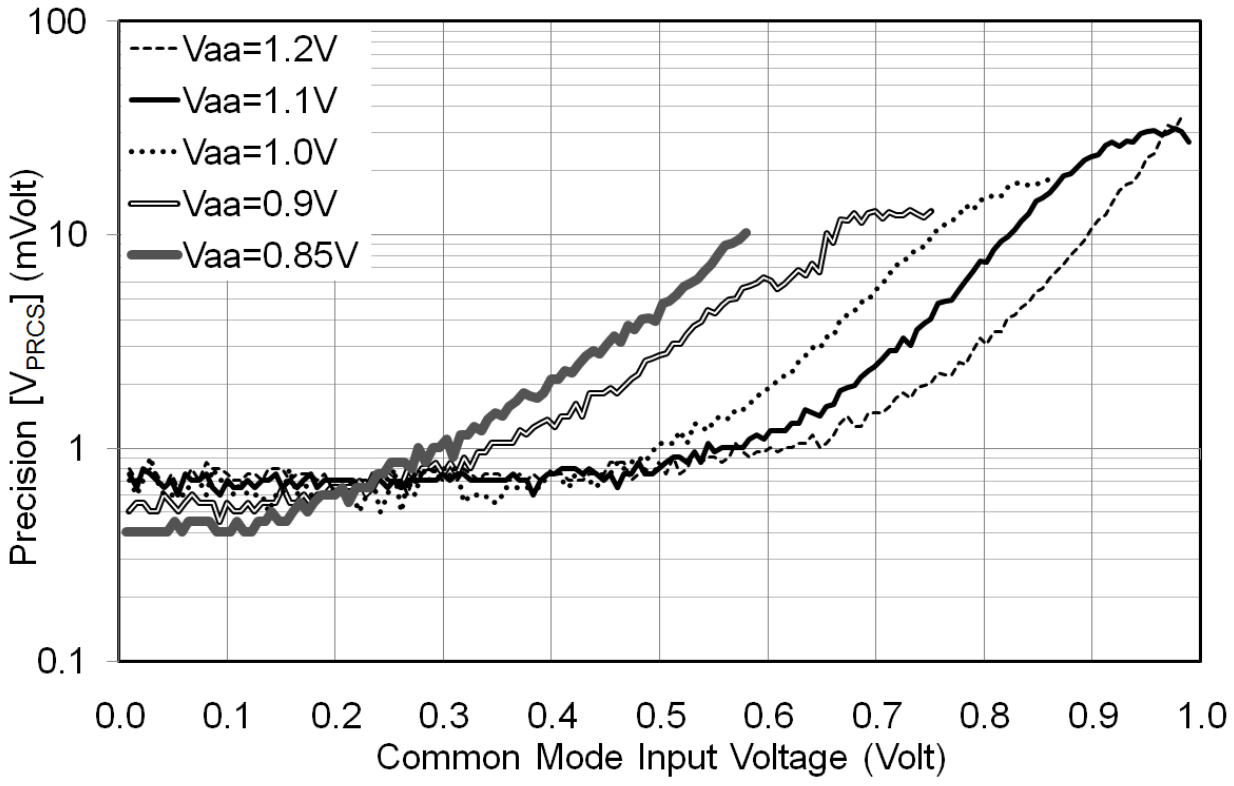
$V_{TH,N}$ = +0.8V
$V_{TH,P}$ = - 0.9V



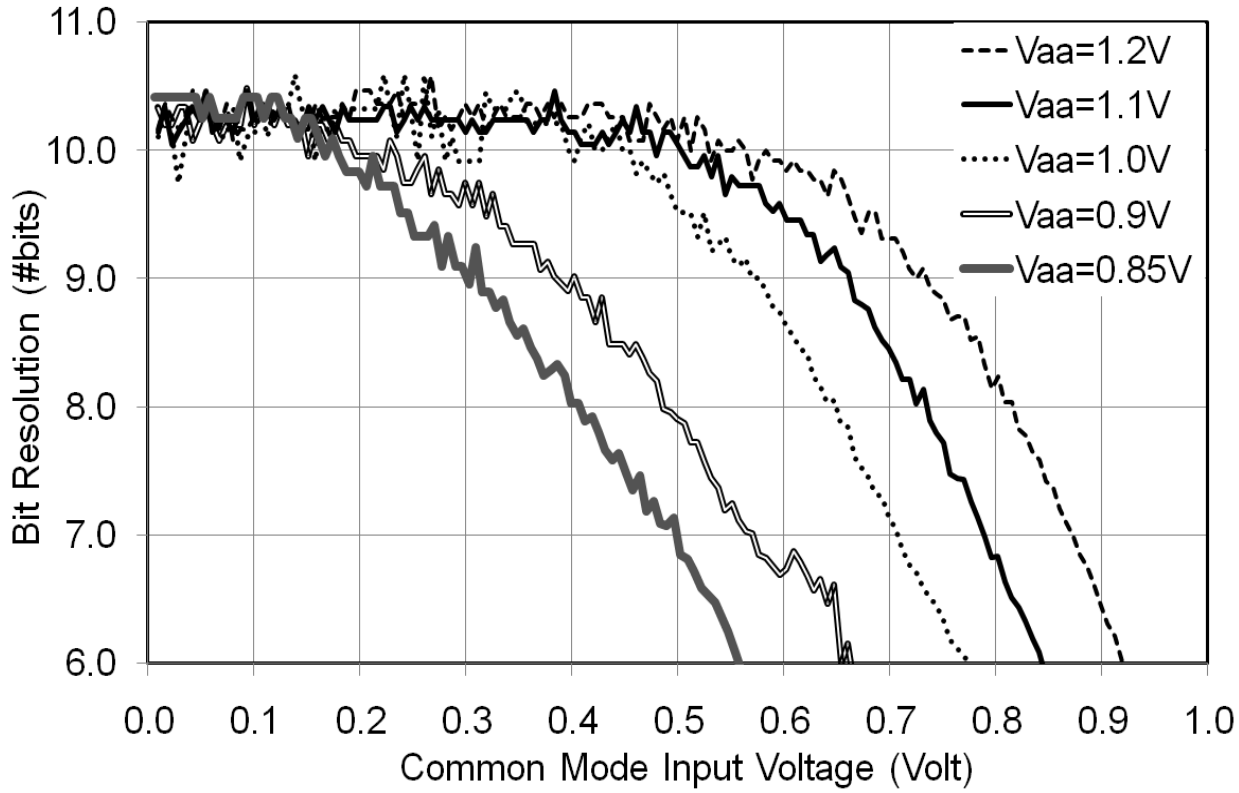
2P3M, 5V, 0.5µm CMOS Process (C5)

Supply Boosted Comparator (Rev.1) – cont.

measured

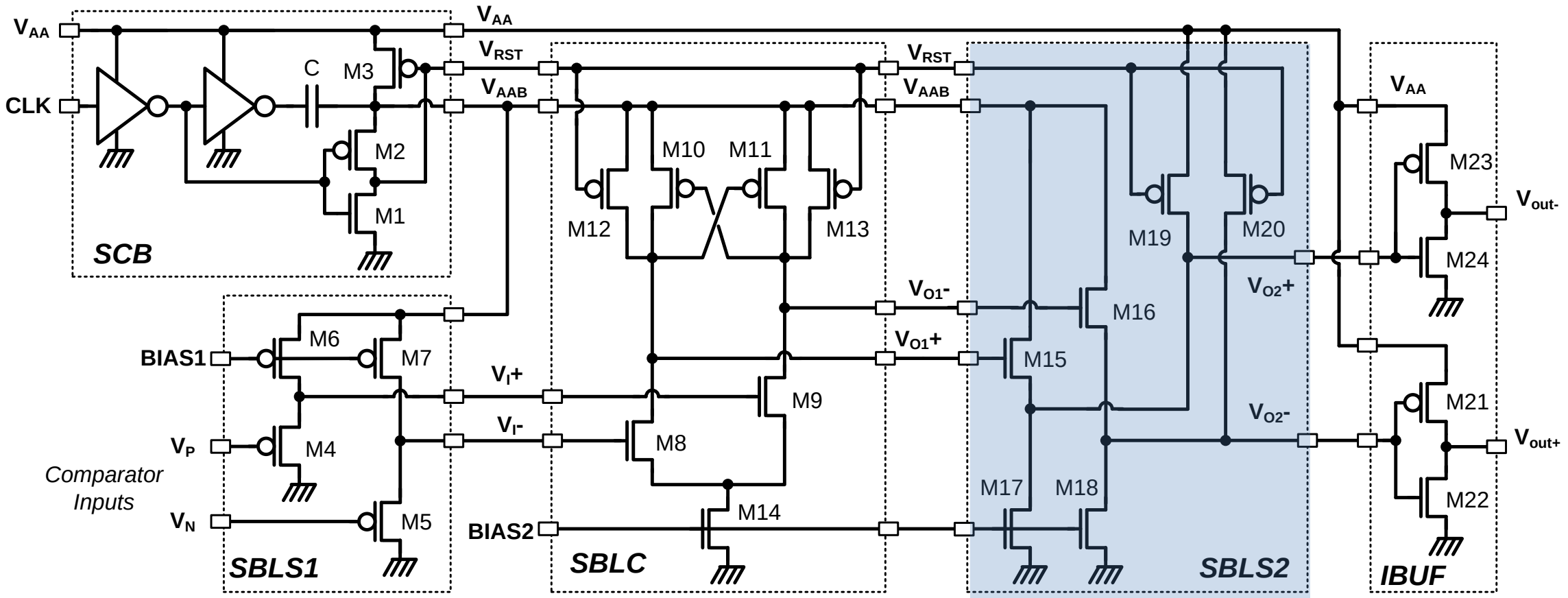


measured



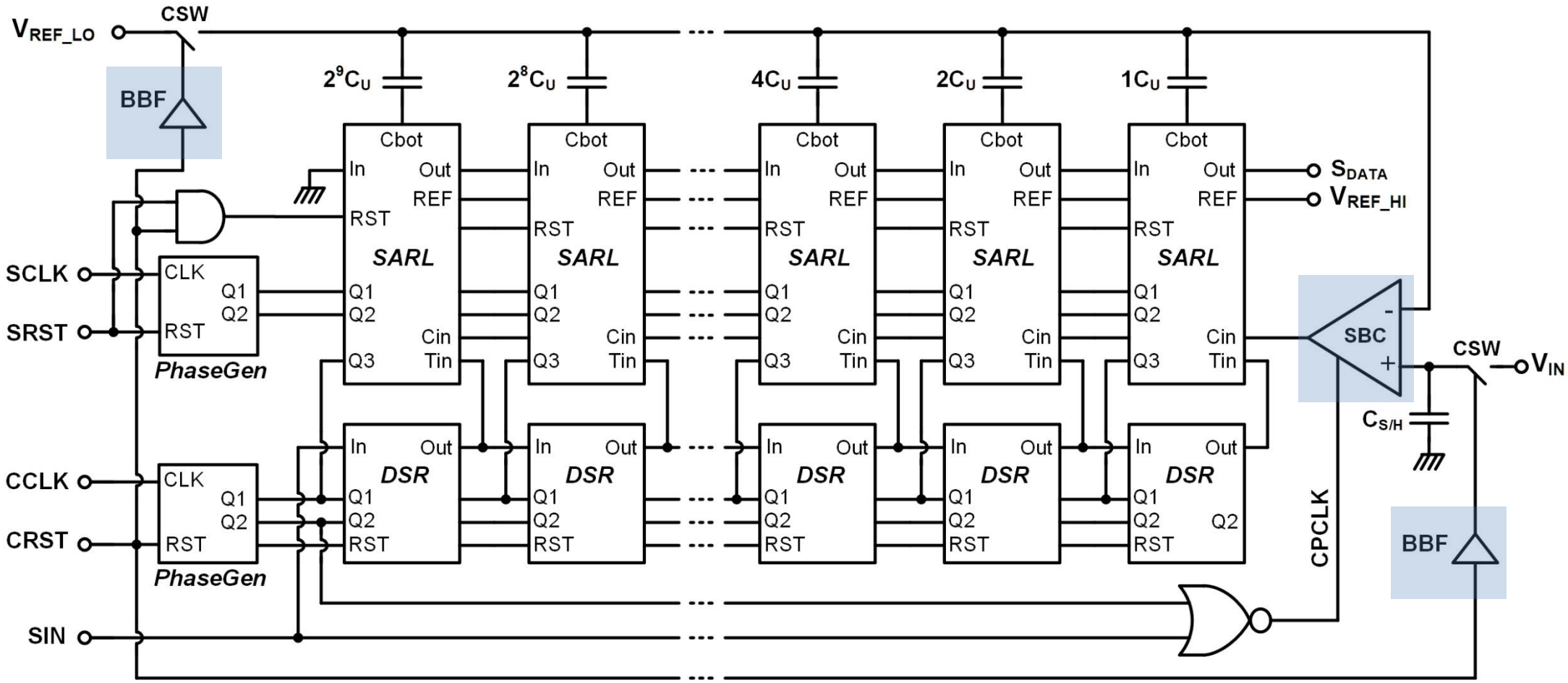
2P3M, 5V, 0.5µm CMOS Process (C5)

Supply Boosted Comparator (Rev.2)

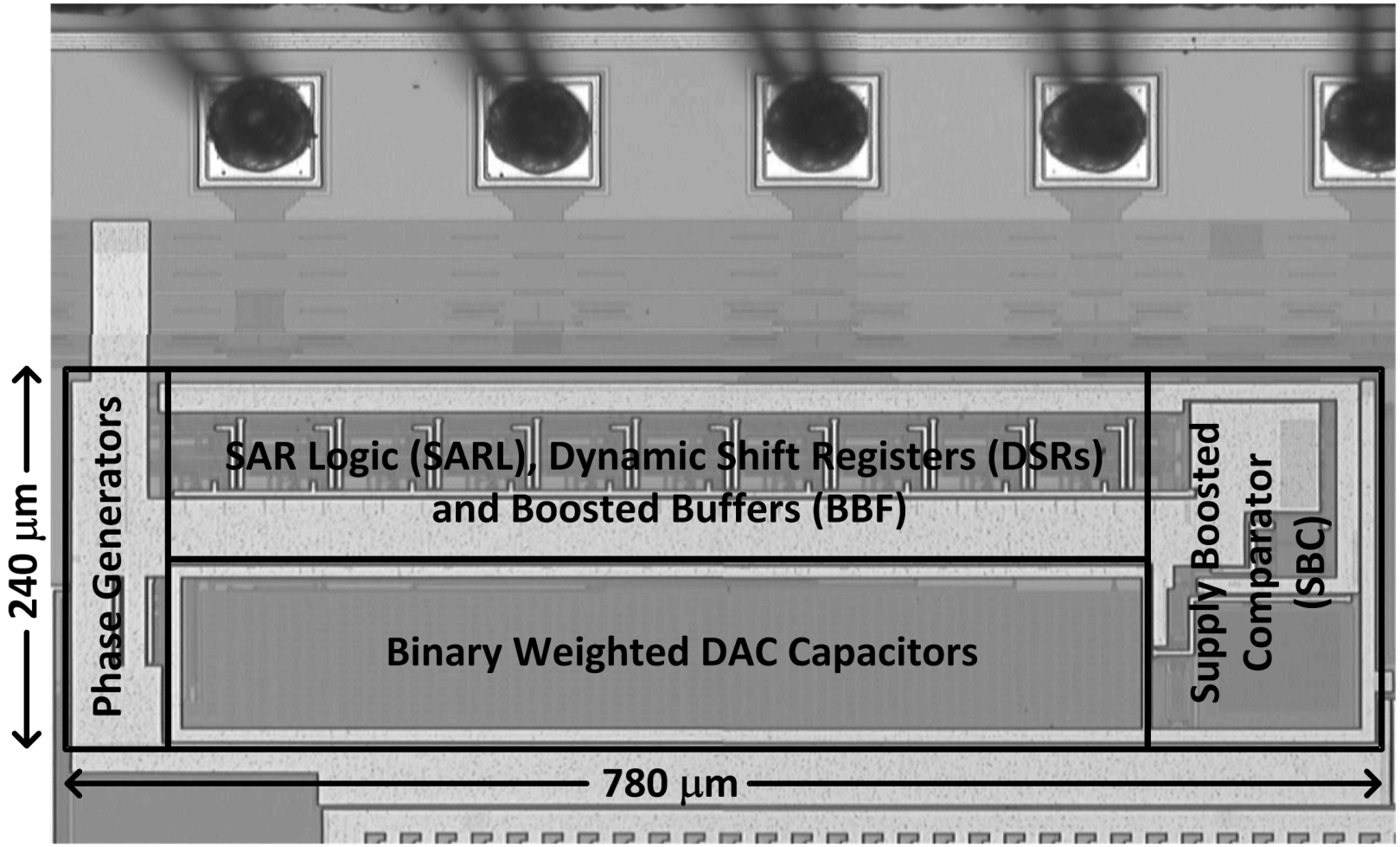


- 100x faster and more energy efficient than the Rev.1

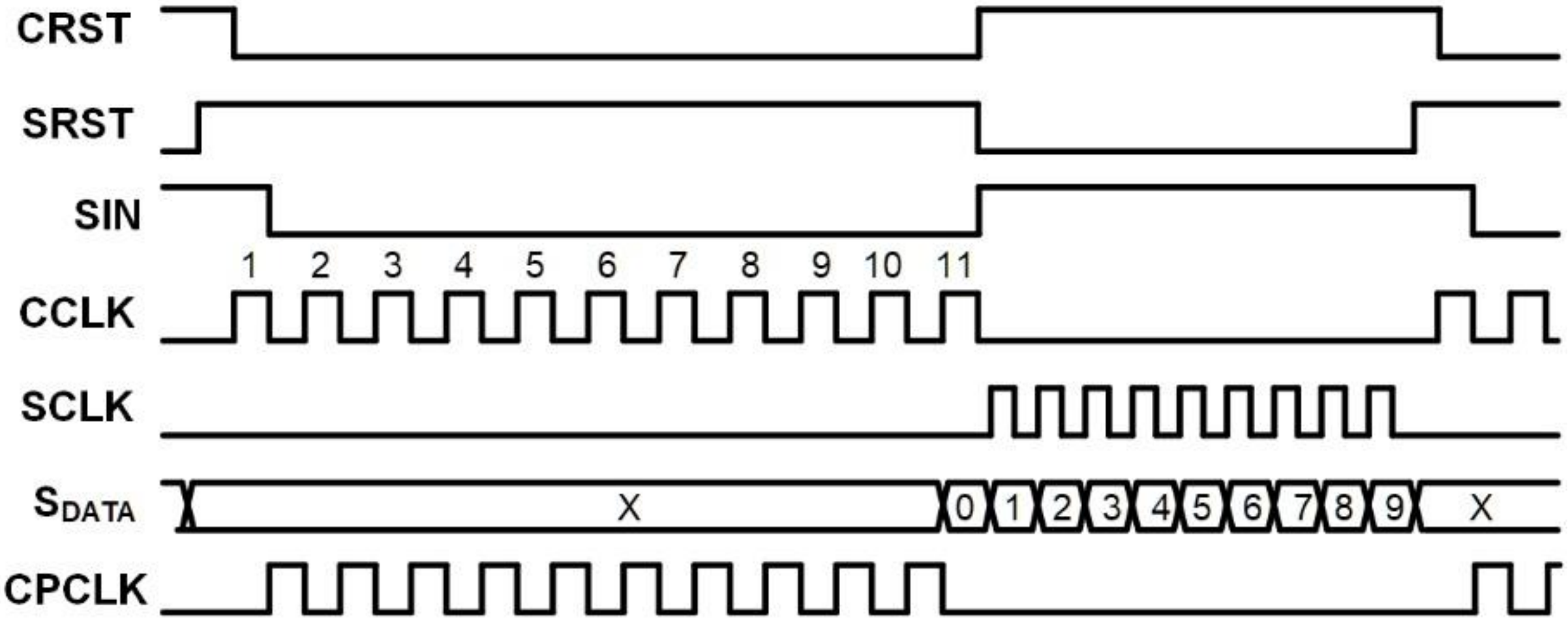
Build SAR ADCs with the SBCs



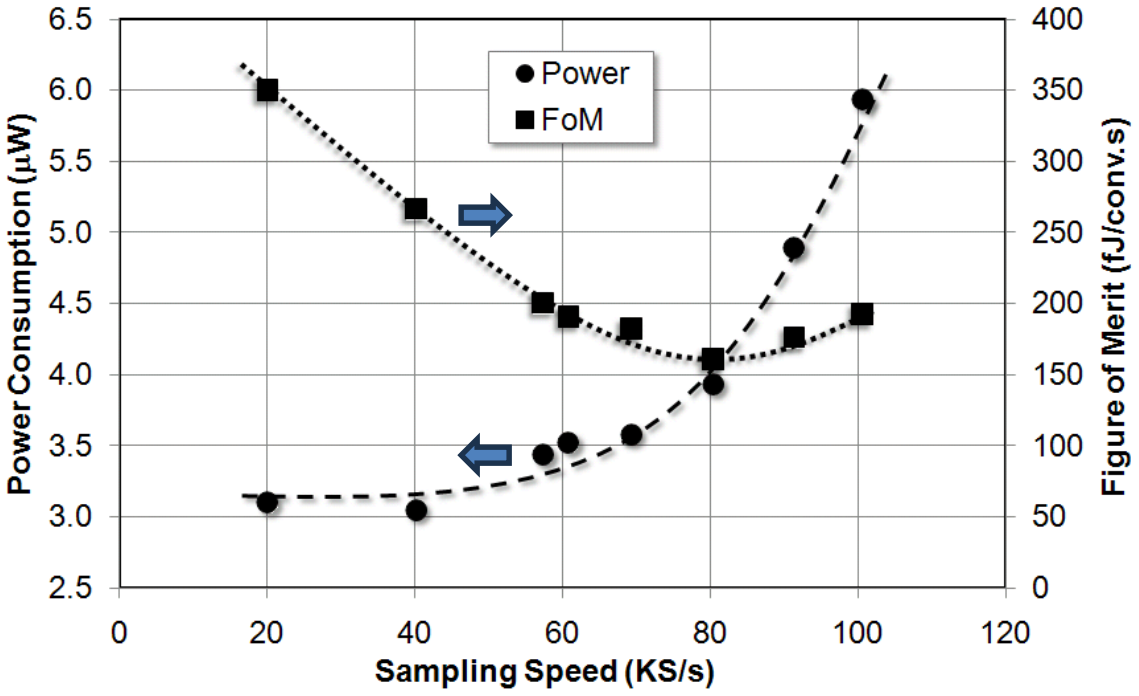
Build SAR ADCs with the SBCs



Build SAR ADCs with the SBCs

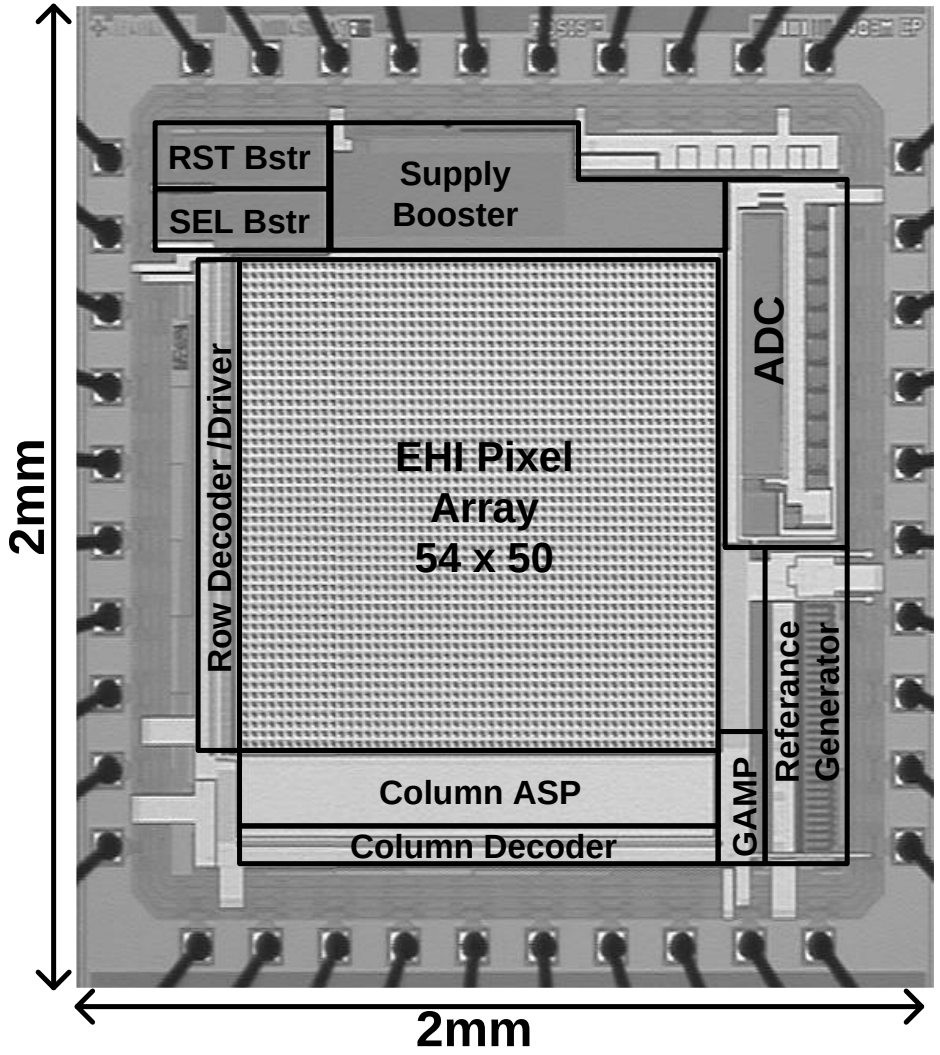


SB ADC Characteristics



Parameter	Value
Resolution	10-bit
Technology	0.5µm CMOS
Supply Voltage	1.2 Volt
Input Range	0.75 Volt
Conversion Speed	80-100 KS/s.
Differential Nonlinearity (DNL)	±0.75 LSB
Integral Nonlinearity (INL)	±2.5 LSB
ENOB	8.24 bits
THD	58.6 dB
SNDR	50.1 dB
SFDR	62.3 dB
Power Consumption	3.95-5.95µW
Figure of Merit (FoM)	163-196 fJ/conv-code
Layout Area	0.187 mm^2

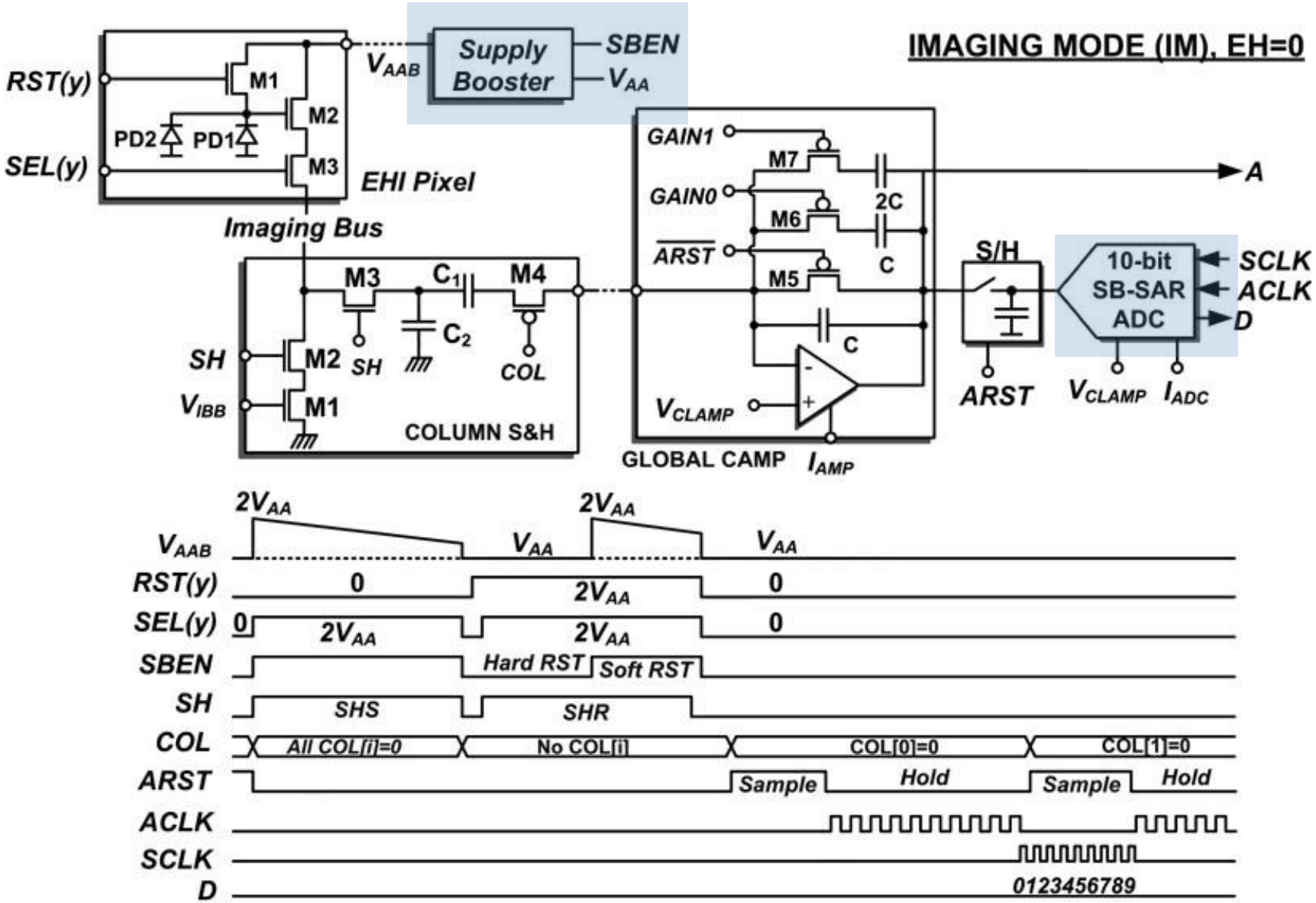
Platform for testing the SBT ideas



- 0.5μm,5V,2P3M CMOS
- 21μm² 3T APS EHI pixels
- 54x50 pixel array
- 2mm x 2mm die area
- Reset/Select/Supply Boosting (RSSB) possible
- Booster caps:
  - C_{supply} = 166pF
  - $C_{rst,sel}$ = 34pF
- SB ADC (10-bit) up to 100KS/s

Intended to be the world's first self-powered CMOS image sensor with energy harvesting capability!

Imaging mode signal path



Power breakdown

V_{AA}=1.2V, 7.4fps, supply boosting enabled for IM

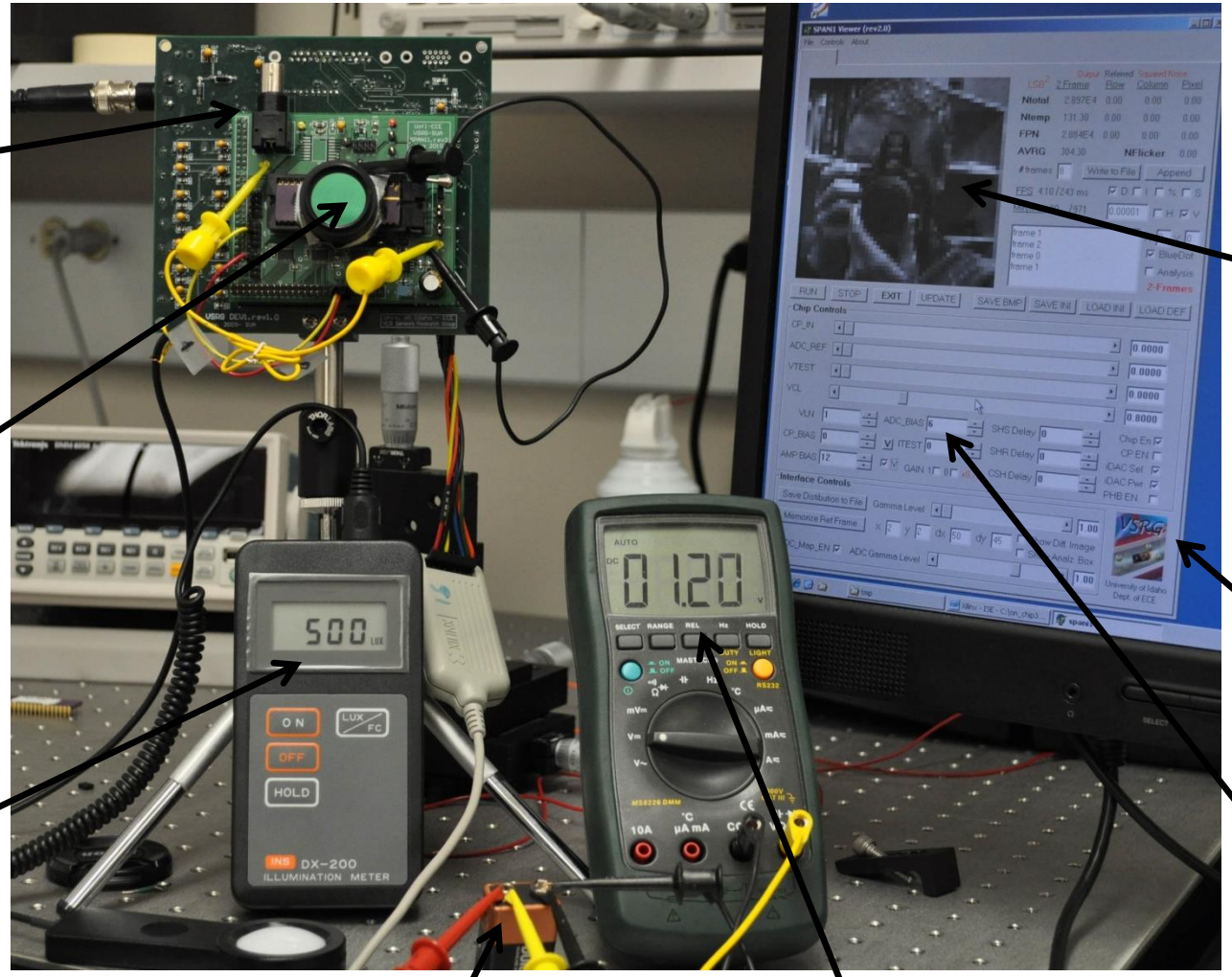
Imaging Mode (IM)	Curent (μA)	Power (μW)
PAD + Charge Pumps + Digital Buffers	4.70	5.64
Referance Generator+ 5 Referance DACs	2.68	3.22
Pixel Array (Pixel SF)	0.022	0.0264
Global Charge Amplifier	1.81	2.17
SB-SAR ADC (Serial Output, 20KS/s)	2.61	3.13
Whole Chip in IM	**11.8**	**14.2**

World's first self-powered CMOS image sensor with solar energy harvesting capability!

8s (harvesting) + 1s (imaging)

S. U. Ay, "A 1.32pW/frame.pixel 1.2V CMOS Energy Harvesting and Imaging (EHI) APS Imager" in 2011 International Solid- State Circuits Conference (ISSCC), pp.116-117, 20-24 February 2011, San Francisco, CA, USA

Demo Setup 1


Test Board
Lens and Green filter
Light Level (500lux)
Captured Video
Test Program
Chip Controls
System Supply (9V)
EHI Supply
500
ON
OFF
HOLD
DX-200
ILLUMINATION METER

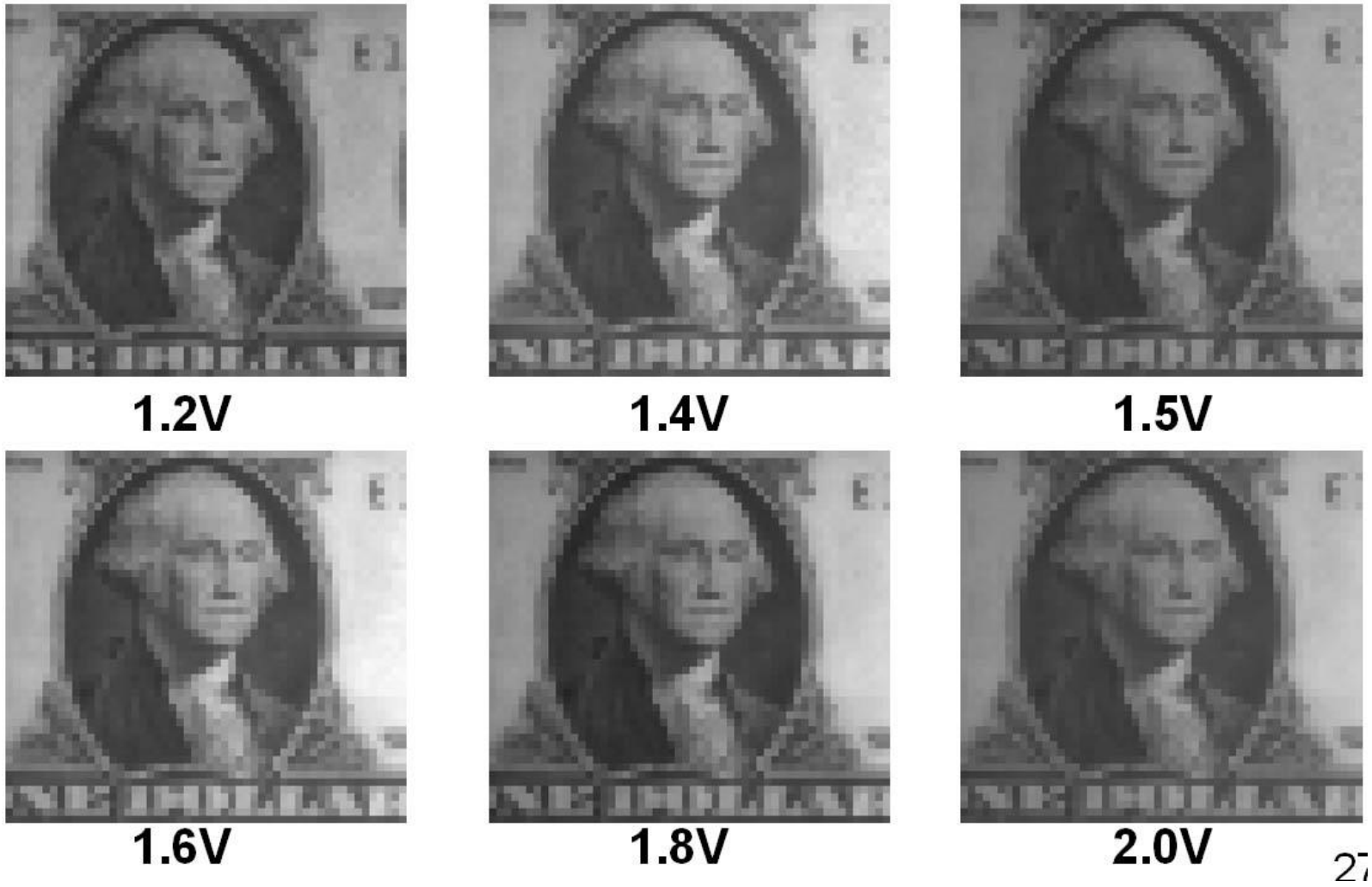
Demo Video 1

Object distance =2.0m, Light=500lux, Vaa=1.2V, 5 FPS

Demo Video 2

Object distance =1.5m, Light=500lux, Vaa=1.2V, 5 FPS

Captured images



– FPN ~0.75%FS @1.5V supply and RSSB operation

Conclusions

- **New and innovative circuit ideas difficult to come by,**
- **Design-by-Analogy (DbA) could help,**
  - Patents are considered to be the best source for inspiration
- **Supply Boosting is a good example for DbA,**
  - It is an ultra low-power design technique
  - It was shown its use in different low power circuit blocks
    - Comparators
    - ADCs
    - CMOS Pixel electronics
  - It made possible to design low-power CMOS imager
- **Need to develop more innovative circuits and design techniques; *any other analogies come to your mind?***

References

Supply Boosting Technique (Comparators, ADCs)

[1] A. Mesgarani, F. Z. Nelson, M. N. Alam, S. U. Ay," Supply Boosting Technique for Designing Very Low-Voltage Mixed-Signal Circuits in Standard CMOS," 53nd IEEE International Midwest Symposium on Circuits and Systems, (MWSCAS),pp.893-896,Seattle, WA, USA,1-4 August,2010.

[2] S. U. Ay, "A sub-1Volt 10-bit Supply Boosted SAR ADC Design in Standard CMOS," Int. Journal on Analog Int. Circuits and Signal Proc., v.66/2, pp.213-221, 2011

[3] A. Mesgarani, S. U. Ay, "A Low Voltage, Energy Efficient Supply Boosted SAR ADC for Biomedical Applications," 2011 IEEE Biomedical Circuits & Systems Conference (BioCAS), San Diego, California November 10-12, pp.4011-404, 2011

[4] S. U. Ay, "Energy Efficient Supply Boosted Comparator Design," Journal of Low Power Electronics and Applications, vol.1, no.2, pp:247-260, 2011.

[5] A. Mesgarani, S. U. Ay, "A 1.2-V 100KS/s Energy Efficient Supply Boosted SAR ADC," in Proc. of IEEE International Midwest Symposium on Circuits and Systems (MWSCAS), page(s): 1152 - 1155, 04-07 August 2013, Columbus, OH, USA.

Supply Boosting Technique (CMOS Image Sensors)

[6] S. U. Ay, "Boosted Readout for CMOS APS Pixels," IEEE International Symposium on Circuits and Systems (ISCAS), pp.2205-2208, 15-18 May, 2011, Rio de Janeiro, Brazil

[7] S. U. Ay, "A 1.32pW/frame.pixel 1.2V CMOS Energy Harvesting and Imaging (EHI) APS Imager" in 2011 International Solid-State Circuits Conference (ISSCC), pp.116-117, 20-24 February 2011, San Francisco, CA, USA

[8] S. U. Ay, "A CMOS Energy Harvesting and Imaging (EHI) Active Pixel Sensor (APS) Imager for Retinal Prosthesis" IEEE Transactions on Biomedical Circuits and Systems, vol. 5, no.6, pp. 535-545, Dec 2011.

[9] S. U. Ay, "Boosted CMOS APS Pixel Readout for Ultra Low-Voltage and Low-Power Operation," IEEE Trans. on Circuits and Systems-II, Vol.60-6, pp. 341-345, June 2013.